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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,577	12/05/2003	Kazutaka Shibata	AI 254 D1	7345

7590 01/10/2006

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,577	SHIBATA, KAZUTAKA	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-8* is/are allowed.

6)☒ Claim(s) *9 and 13-16* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/05/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on 31 October 2005.

2. Currently, claims 5-16 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 9 and 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Gupta et al. (US 2005/0224921 A1).

The Gupta et al. pre-grant published application (Gupta) discloses a method for manufacturing a semiconductor device (figs. 1, 8-11 and accompanying text). The method includes: connecting face down a semiconductor chip 202 having an active surface with a recess and a conductor 210 disposed in the recess onto one surface 201 of a semiconductor substrate (fig. 8 and par. 30, lines 1-13); and polishing or abrading an inactive surface of the semiconductor chip to expose the conductor 210 in the inactive surface of the semiconductor chip after the on-substrate connecting step (fig. 9; par. 31, lines 1-4; and par. 31, lines 10-13).

Another semiconductor chip can be connected onto the semiconductor chip, wherein the other semiconductor chip has an active surface formed with a recess and a conductor therein, and is connected face down on to the semiconductor chip 202 (figs. 1, 11; par. 33, lines 1-4; and par. 33, lines 6-11). A polishing or abrading step is performed in an inactive surface of the other semiconductor chip to expose the conductor therein at the inactive surface (par. 33, lines 11-13).

Furthermore, Gupta discloses a method for manufacturing a semiconductor device (figs. 1, 8-11 and accompanying text), wherein the method includes: a step of connecting a semiconductor chip on an active surface of a semiconductor substrate 203 having an active surface formed with a recess having a conductor 210 therein (fig. 8 and par. 30, lines 1-13); and a step of polishing or abrading an inactive surface of the semiconductor substrate 203 to expose the conductor 210 (fig. 9; par. 31, lines 1-4; and par. 31, lines 10-13).

Allowable Subject Matter

4. Claims 5-8 are allowable over the prior art of record. The prior art of record does not anticipate, teach or suggest a method for manufacturing a semiconductor device substantially as claimed, wherein the method comprises: connecting, to one surface of a support semiconductor chip, first and second chip blocks each including one or a plurality of semiconductor chips having an active surface substantially parallel with the one surface of the support

semiconductor chip; and arranging an insulator at between the first and second chip blocks.

5. Claims 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. The amendment filed on 31 October 2005 has overcome the 35 USC 112, second paragraph rejection made of record in the Office action mailed on 30 June 2005. Accordingly, the rejection is withdrawn.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
08 January 2006

Mary Wilczewski
Primary Examiner